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Harmonic Analysis of Three Level Diode Clamped Inverter

Pooja Sahastrabuddhe
Student
Department of Electrical Engineering
Tulasiramji Gaikwad-Patil College of Engineering & Technology, Nagpur, India

Dr. Hari Kumar Naidu
Dean
Department of Electrical Engineering
Tulasiramji Gaikwad-Patil College of Engineering & Technology, Nagpur, India

Abstract

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. Multilevel inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages. In order to maintain the different voltage levels at appropriate intervals, the conduction time intervals of MOSFETS have been maintained by controlling the pulse width of gating pulses. In this paper single phase to three phase power conversion using PWM technique. The simulation is carried out in MATLAB/Simulink environment which demonstrate the feasibility of proposed scheme.
Keywords: Inverter, Microcontroller, MOSFET, Pulse Width Modulation

I. INTRODUCTION

Over the years, three-phase motors, more than single phase motors have been the main consideration in industries due to certain parameters such as; efficiency, torque ripples and power factor. In rural areas, in order to operate machine tools and rolling mills as well as in low power industrial application for robotics, where a three phase utility may not be available, high-performance converters are typically used to run the three-phase motor drives. Low losses and cost effectiveness are the very important properties for these converters various single-phase to three-phase converters have been proposed with at least 6 switches. An alternative for the reduction of losses in these converters is that the number of power switches is reduced. Many components-minimized structures are proposed in literatures[1]

Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped) capacitor- clamped (flying capacitors) and cascaded multi cell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).[7 8]

The most attractive features of multilevel inverters are as follows.

1) They can generate output voltages with extremely low distortion and lower dv/dt.
2) They draw input current with very low distortion.
3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
4) They can operate with a lower switching frequency. The diode-clamp method can be applied to higher level converters

As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion. Ultimately, a zero harmonic distortion of the output wave can be obtained by an infinite number of levels. More levels also mean higher voltages can be spanned by series devices without device voltage sharing problems. [9 10] Unfortunately, the number of the achievable voltage levels is quite limited not only due to voltage unbalance problems but also due to voltage clamping requirement, circuit layout, and packaging constraints.

The simulation is carried out in Matlab/Simulink environment which demonstrate the feasibility of proposed scheme.

II. DIODE CLAMPED MULTILEVEL CONVERTER

Three-level diode-clamped inverter is shown in Fig. 1. In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 & C_2. The middle point of the two capacitors can be defined as the neutral point. The output voltage v_{an} has three states: $V_{dc}/2$ and $-V_{dc}/2$. For voltage level $V_{dc}/2$, switchesS_1 and S_2 need to be turned on; for$-V_{dc}/2$, switchesS_1' and S_2' need to be turned on; and for the 0 level, S_2 and S_1' need to be turned on. The key components that distinguish this circuit from a conventional two-level inverter are D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both $S_1$and S_2 turn on, the voltage across a and 0 is, i.e., $v_{ao}=V_{dc}$. In this case, D_1' balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across $C_1$and S_2' blocking the voltage acrossC_2.

Output voltage v_{an} is ac, and v_{ao} is dc. The difference between v_{an} and v_{ao} is the voltage across C_2, which is $V_{dc}/2$. If the output is removed out between a and 0, then the circuit becomes a dc/dc converter, which has three output voltage levels: V_{dc}, $V_{dc}/2$ and 0.

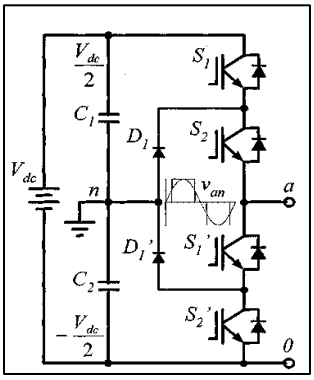

Fig. 1: Three level diode clamped inverter

III. CONTROL TECHNIQUE OF DIODE CLAMPED MULTILEVEL INVERTER

The sinusoidal PWM technique is very popular for industrial converters. In this technique, an isosceles triangle carrier wave of frequency fc is compared with the fundamental frequency f sinusoidal modulating wave and the points of intersection determines the switching points of power devices.

Two important parameters of the design process are amplitude modulation index ma= Vr/Vc, where Vr is the peak amplitude of reference control signals, Vc is the peak amplitude of the carrier wave, and the frequency modulation index mf= fc/fr, where fc is the frequency of the carrier wave and fr is the reference sinusoidal signal frequency. Ma and fr determines the magnitude and frequency of output voltage, fc determines switching frequency of power semiconductor devices.

Multilevel converters are mainly controlled with sinusoidal PWM extended to multiple carrier arrangements of two types: Level Shifted (LS-PWM), which includes Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM) and Alternative Phase Opposition Disposition (APOD-PWM) or they can be Phase Shifted (PS-PWM). In present topology PD is used.

IV. PROPOSE SCHEME

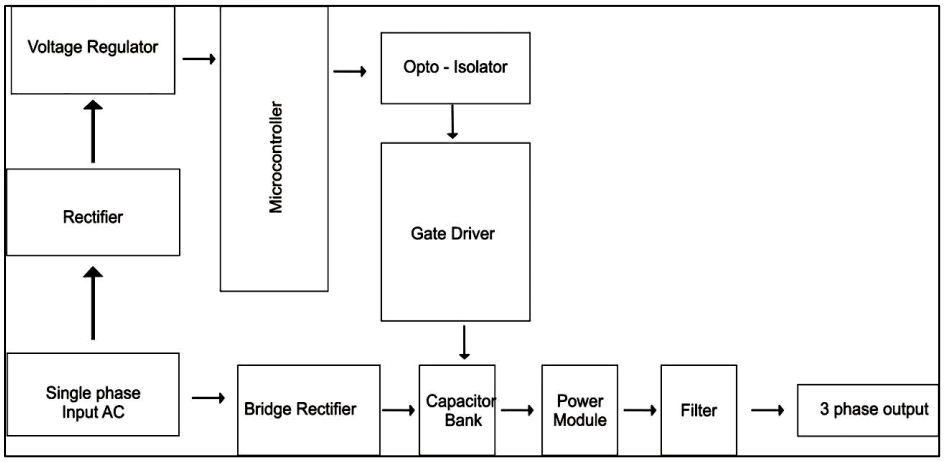

Fig. 2: Block Diagram of Single Phase to Three Phase Conversion

The proposed scheme describes the theory of 1 phase to 3 phase conversion and the hardware implementation shall be made using a programmed microcontroller of 8051 family duly interfaced to 3 phase inverter with 6 number MOSFET or IGBTs from DC derived from a single phase, 50 Hz supply. The load can be a star connected three phase 50 Hz, 440 volt, 0.5 to 1 HP motor. Alternatively, a star lamp load can be used to view the waveform only. The power supply consists of a step down transformer 230/12V, which steps down the volt a to 12V AC. This is converted to DC using a Bridge rectifier. The ripples are removed using a capacitive filter and it is then regulated to +5V using a voltage regulator 7805 which is required for the operation of the microcontroller and other components.

V. HARDWARE IMPLEMENTATION

The figure shows the hardware implementation of project single phase to three phase power conversion by PWM technique. There are twelve MOSFET's are used for three level inverter.

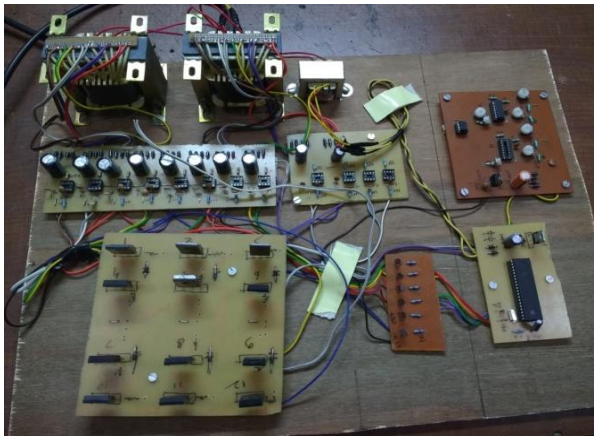

Fig. 3: Hardware Implementation

VI. MULTILEVEL PWM INVERTER

The multilevel PWM inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages in stepped waveform. The commutation of the switches allows the addition of the capacitor voltages which reaches the high voltage level at the output, while the power semiconductors withstand only with reduced voltage. A five-level PWM inverter generates an output voltage with five values (levels) with respect to the negative terminal of the capacitor. By considering that 'n' is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load 'K' is defined by:

$$K = 2m + 1 \quad \ldots(1)$$

The number of steps p in the phase voltage of a single-phase load in wyes connection is given by:

$$p = 2k+1 \quad \ldots (2)$$

The term multilevel starts with the three-level inverter. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, it results to reduction in harmonic distortion. However, a high number of levels results in increasing the complexity and also introduce voltage imbalance problems.

Three different topologies have been proposed for multilevel inverters as diode-clamped (neutral-clamped), capacitor Clamped (flying capacitors) and cascaded multicell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination and space-vector modulation (SVM).

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VII. MOSFET DRIVER

It is beneficial to use N-channel MOSFETs as the high side switches as well as the low side switches because they have a lower 'ON' resistance and therefore less power loss. However, to do so, the drain of the high side device is connected to the 170V DC power which is to be inverted into the 120 AC power. This is a problem because the 170V is the highest voltage in the system and in order for the switch to be turned on the voltage at the gate terminal must be 10V higher than the drain terminal voltage. In order to achieve the extra voltage necessary to switch on the device, a MOSFET driver is used with a bootstrap capacitor.

The MOSFET driver operates from a signal input given from the microcontroller and takes its power from the battery voltage supply that the system uses. The driver is capable of operating both the high side and low side devices, but in order to get the extra 10V for the high side device, an external bootstrap capacitor is charged through a diode from the 12V power supply when the device is off. Because the power for the driver is supplied from the low voltage source, the power consumed to drive the gate is small. When the driver is given the signal to turn on the high side device, the gate of the MOSFET has an extra boost in charge from the bootstrap capacitor, surpassing the needed 10V to activate the device and turning the

VIII. MICROCONTROLLER

In order to use the H-bridge properly, there are four MOSFETs that need to be controlled. This can be done either with analog circuits or a microcontroller. In this case, we chose the microcontroller over the analog system for several reasons. First, it would

be simpler to adapt. With an analog system, it would be difficult to make changes for the desired output. In many cases, this is a desired trait, as it would be designed for a single purpose and therefore a single output. However, as this is something that is designed to be available all over the world, it needs to be adjustable to different standards of frequency and voltage. With an analog circuit, this would require a different circuit that it would have to switch over to, while with a micro-controller, it merely requires a change in the program's code. The second advantage of using a microcontroller is that it can allow for easy feedback to control the power flowing through the load. One of the problems that can occur with systems like this is that the variances in load can cause variances in the supplied current and voltage. With a microcontroller, it is possible to have it "look" at the power output and change the duty cycle based on whether or not the load requires additional power or is being oversupplied.

Necessary waveforms generated by the microcontroller v_{ao}, v_{bo}, v_{co} and the ouput v_{ab}, v_{bc}, v_{ca}.

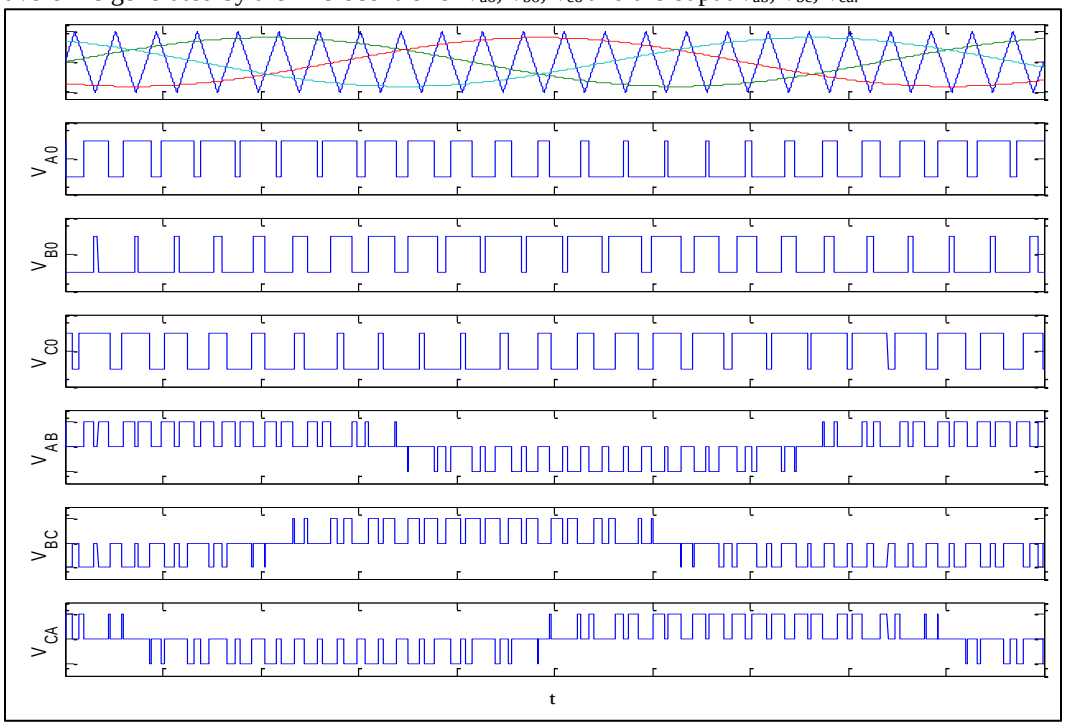

Fig. 4: Microcontroller

IX. SIMULATION RESULTS

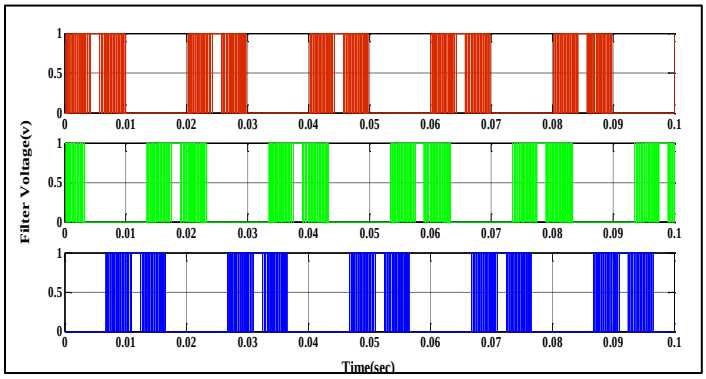

Fig. 5: Input DC Voltage

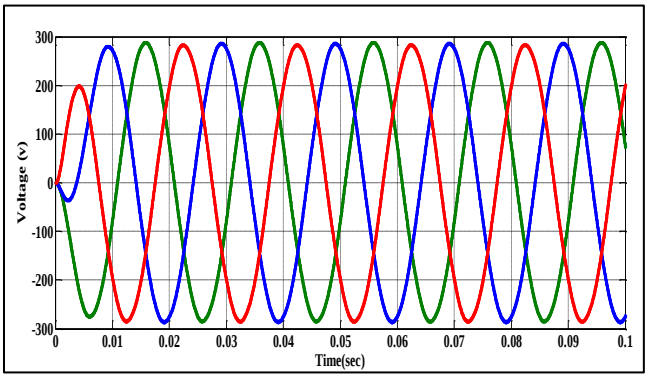

Fig. 6: Three Phase Sinosoidal Voltage

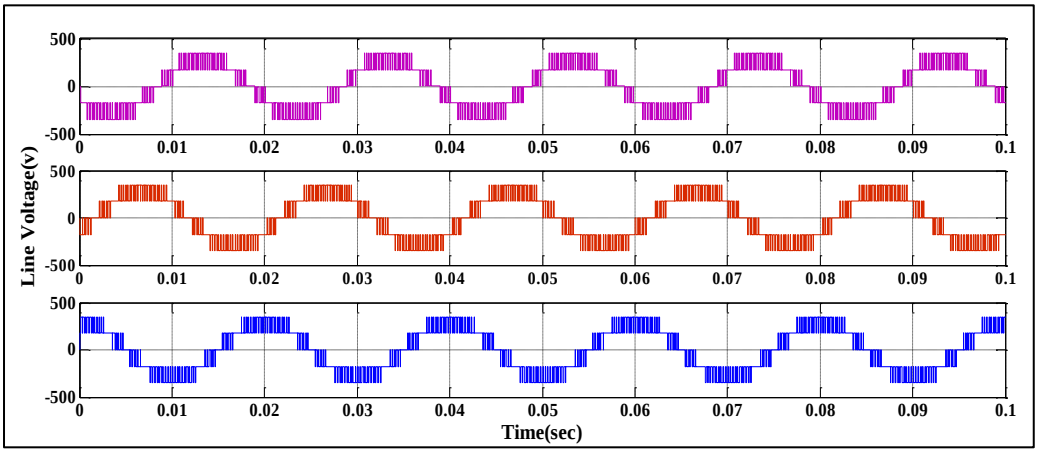

Fig. 7: Three Level Output Voltage

The input dc voltage and three phase sinusoidal voltage is shown in fig.3and fig.4. The output result of three level diode clamped inverter is shown in fig.5 It is observed that there is phase of 120 degree in three phase voltage.

X. TOTAL HARMONIC DISTORTION

From Three Level Inverter output waveform three levels i.e. -200V, 0V and +200V of output voltage is obtained. The CMV varies from -200V to +200V can be observed from waveform of CMV of Three Level Inverter. From FFT analysis THD is obtained 34.88% in Line Voltage of Two Level Inverter. Here, CMV is decreases from CMV of Two Level Inverter and is also decrease as compare to Two Level Inverter. As the comparison with 2-level inverter reduction in THD is shown in the graph below.

Modulation Index (ma)	*% THD 2-Level*	*% THD 3-Level*	*% Reduction in THD*
1.1	*31.94*	*15.93*	*50%*
1	*35.25*	*17.23*	*51%*
0.9	*39.20*	*17.45*	*54%*
0.8	*42.03*	*21.73*	*56%*
0.7	*44.30*	*24.18*	*57%*
0.6	*49.17*	*26.43*	*58%*
0.5	*68.54*	*34.38*	*60%*

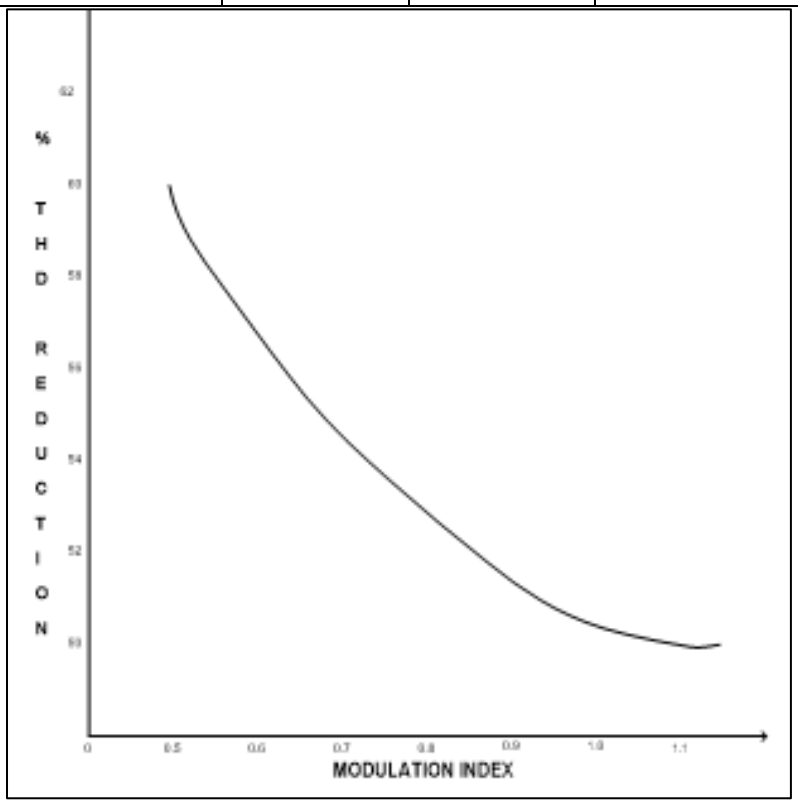

Fig. 6: Reduction in THD

XI. CONCLUSION

In this paper diode clamped Multilevel Inverter required only two-battery sources. A three level equal step switching control has been applied to obtain a multilevel ac output. Multilevel Inverter with unequal voltage sources is simulated using MATLAB Simulink. This paper presents a single-phase to three-phase conversion system that improves the local power quality for linear and non-linear loads, and guarantees unity power factor at the single-phase feeder. The inverter controls the local power quality, producing three-phase, symmetrical and sinusoidal voltages. It also controls the single-phase power flow, by adjusting the local voltage amplitude and phase angle.

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